

MC10E137, MC100E137

5 V ECL 8-Bit Ripple Counter

Description

The MC10E/100E137 is a very high speed binary ripple counter. The two least significant bits were designed with very fast edge rates while the more significant bits maintain standard ECLinPS™ output edge rates. This allows the counter to operate at very high frequencies while maintaining a moderate power dissipation level.

The device is ideally suited for multiple frequency clock generation as well as a counter in a high performance ATE time measurement board.

Both asynchronous and synchronous enables are available to maximize the device's flexibility for various applications. The asynchronous enable input, A_Start, when asserted enables the counter while overriding any synchronous enable signals. The E137 features XORed enable inputs, EN1 and EN2, which are synchronous to the CLK input. When only one synchronous enable is asserted the counter becomes disabled on the next CLK transition; all outputs remain in the previous state poised for the other synchronous enable or A_Start to be asserted to re-enable the counter. Asserting both synchronous enables causes the counter to become enabled on the next transition of the CLK. If EN1 (or EN2) and CLK edges are coincident, sufficient delay has been inserted in the CLK path (to compensate for the XOR gate delay and the internal D-flip flop setup time) to insure that the synchronous enable signal is clocked correctly, hence, the counter is disabled.

All input pins left open will be pulled LOW via an input pulldown resistor. Therefore, do not leave the differential CLK inputs open. Doing so causes the current source transistor of the input clock gate to become saturated, thus upsetting the internal bias regulators and jeopardizing the stability of the device.

The asynchronous Master Reset resets the counter to an all zero state upon assertion.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The 100 Series contains temperature compensation.

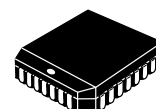
Features

- Differential Clock Input and Data Output Pins
- V_{BB} Output for Single-Ended Use
- Synchronous and Asynchronous Enable Pins
- Asynchronous Master Reset
- PECL Mode Operating Range:
 - ♦ V_{CC} = 4.2 V to 5.7 V with V_{EE} = 0 V
- NECL Mode Operating Range:
 - ♦ V_{CC} = 0 V with V_{EE} = -4.2 V to -5.7 V
- Internal Input 50 kΩ Pull-down Resistors
- Transistor Count = 330 devices
- ESD Protection:



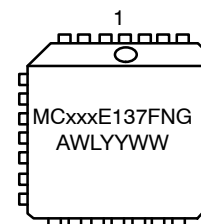
ON Semiconductor®

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PLCC-28
FN SUFFIX
CASE 776-02

MARKING DIAGRAM*



xxx = 10 or 100
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

*For additional marking information, refer to Application Note [AND8002/D](#).

ORDERING INFORMATION

| Device | Package | Shipping† |
|--------------|----------------------|---------------|
| MC10E137FNG | PLCC-28 (Pb-Free) | 37 Units/Tube |
| MC100E137FNG | PLCC-28 (Pb-Free) | 37 Units/Tube |

- ♦ Human Body Model: > 2 kV
- ♦ Machine Model: > 200 V
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level: 3 (Pb-Free)
 - ♦ For Additional Information, see Application Note [AND8003/D](#)
- Flammability Rating: UL 94 V-0 @ 0.125 in, Oxygen Index: 28 to 34
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

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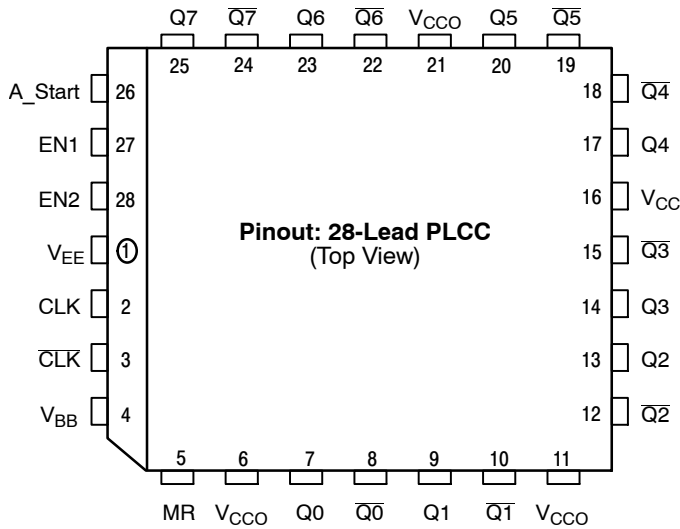


Table 1. PIN DESCRIPTION

| PIN | FUNCTION |
|------------------------------------|-------------------------------|
| CLK, $\overline{\text{CLK}}$ | ECL Differential Clock Inputs |
| Q0-Q7, $\overline{\text{Q0-Q7}}$ | ECL Differential Q Outputs |
| A_Start | ECL Asynchronous Enable Input |
| EN1, EN2 | ECL Synchronous Enable Inputs |
| MR | Asynchronous Master Reset |
| V _{BB} | Reference Voltage Output |
| V _{CC} , V _{CCO} | Positive Supply |
| V _{EE} | Negative Supply |

* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. 28-Lead Pinout

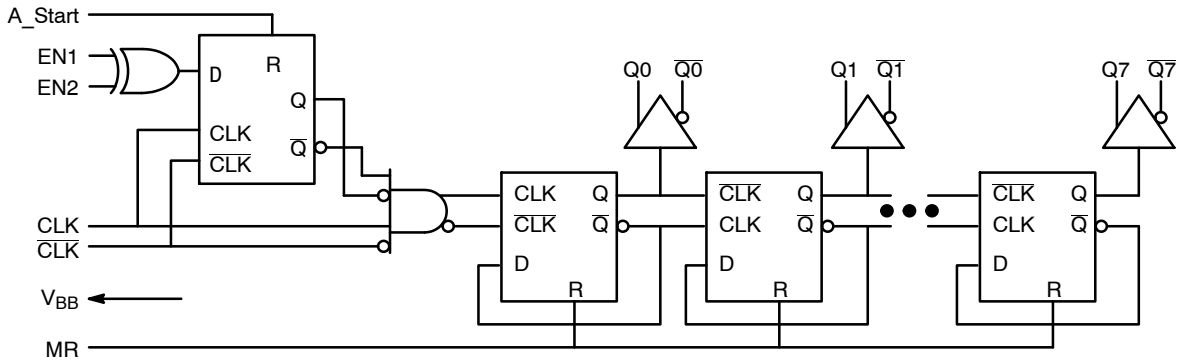


Figure 2. Logic Diagram

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Table 2. SEQUENTIAL TRUTH TABLE

| Function | EN1 | EN2 | A_Start | MR | CLK | Q7 | Q6 | Q5 | Q4 | Q3 | Q2 | Q1 | Q0 |
|--------------|-----|-----|---------|----|-----|----|----|----|----|----|----|----|----|
| Reset | X | X | X | H | X | L | L | L | L | L | L | L | L |
| Count | L | L | L | L | Z | L | L | L | L | L | L | L | H |
| | L | L | L | L | Z | L | L | L | L | L | L | H | L |
| | L | L | L | L | Z | L | L | L | L | L | L | H | H |
| Stop | H | L | L | L | Z | L | L | L | L | L | L | H | H |
| | H | L | L | L | Z | L | L | L | L | L | L | H | H |
| Asynch Start | H | L | H | L | Z | L | L | L | L | L | H | L | L |
| | H | L | H | L | Z | L | L | L | L | L | H | L | H |
| | L | L | H | L | Z | L | L | L | L | L | H | H | L |
| Count | L | L | L | L | Z | L | L | L | L | L | H | H | H |
| | L | L | L | L | Z | L | L | L | L | H | L | L | L |
| | L | L | L | L | Z | L | L | L | L | H | L | L | H |
| Stop | L | H | L | L | Z | L | L | L | L | H | L | L | H |
| | L | H | L | L | Z | L | L | L | L | H | L | L | H |
| Synch Start | H | H | L | L | Z | L | L | L | L | H | L | H | L |
| | H | H | L | L | Z | L | L | L | L | H | L | H | H |
| | H | H | L | L | Z | L | L | L | L | H | H | L | L |
| Stop | H | L | L | L | Z | L | L | L | L | H | H | L | L |
| | H | L | L | L | Z | L | L | L | L | H | H | L | L |
| Count | L | L | L | L | Z | L | L | L | L | H | H | L | H |
| | L | L | L | L | Z | L | L | L | L | H | H | H | L |
| | L | L | L | L | Z | L | L | L | L | H | H | H | H |
| Reset | X | X | X | H | X | L | L | L | L | L | L | L | L |

Z = Low to High Transition

Table 3. MAXIMUM RATINGS

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|------------------|--|--|--|----------------------------|------|
| V _{CC} | PECL Mode Power Supply | V _{EE} = 0 V | | 8 | V |
| V _{EE} | NECL Mode Power Supply | V _{CC} = 0 V | | -8 | V |
| V _I | PECL Mode Input Voltage NECL Mode Input Voltage | V _{EE} = 0 V V _{CC} = 0 V | V _I ≤ V _{CC} V _I ≥ V _{EE} | 6 -6 | V |
| I _{out} | Output Current | Continuous Surge | | 50 100 | mA |
| T _A | Operating Temperature Range | | | 0 to +85 | °C |
| T _{stg} | Storage Temperature Range | | | -65 to +150 | °C |
| θ _{JA} | Thermal Resistance (Junction-to-Ambient) | 0 lfpm 500 lfpm | PLCC-28 | 63.5 43.5 | °C/W |
| θ _{JC} | Thermal Resistance (Junction-to-Case) | Standard Board | PLCC-28 | 22 to 26 | °C/W |
| V _{EE} | PECL Operating Range NECL Operating Range | | | 4.2 to 5.7 -5.7 to -4.2 | V |
| T _{sol} | Wave Solder (Pb-Free) | | | 265 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

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Table 4. 10E SERIES PECL DC CHARACTERISTICS ($V_{CCx} = 5.0\text{ V}$; $V_{EE} = 0.0\text{ V}$ (Note 1))

| Symbol | Characteristic | 0°C | | | 25°C | | | 85°C | | | Unit |
|-------------|--|------|----------|------|------|------|------|------|------|------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | | 121 | 145 | | 121 | 145 | | 121 | 145 | mA |
| V_{OH} | Output HIGH Voltage (Note 2) | 3980 | 40 70 | 4160 | 4020 | 4105 | 4190 | 4090 | 4185 | 4280 | mV |
| V_{OL} | Output LOW Voltage (Note 2) | 3050 | 3210 | 3370 | 3050 | 3210 | 3370 | 3050 | 3227 | 3405 | mV |
| V_{IH} | Input HIGH Voltage (Single-Ended) | 3830 | 3995 | 4160 | 3870 | 4030 | 4190 | 3940 | 4110 | 4280 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) | 3050 | 3285 | 3520 | 3050 | 3285 | 3520 | 3050 | 3302 | 3555 | mV |
| V_{BB} | Output Voltage Reference | 3.62 | | 3.73 | 3.65 | | 3.75 | 3.69 | | 3.81 | V |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3) | 2.2 | | 4.6 | 2.2 | | 4.6 | 2.2 | | 4.6 | V |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current | 0.5 | 0.3 | | 0.5 | 0.25 | | 0.3 | 0.2 | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary $-0.46\text{ V} / +0.06\text{ V}$.
2. Outputs are terminated through a $50\ \Omega$ resistor to $V_{CC} - 2.0\text{ V}$.
3. V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} .

Table 5. 10E SERIES NECL DC CHARACTERISTICS ($V_{CCx} = 0.0\text{ V}$; $V_{EE} = -5.0\text{ V}$ (Note 1))

| Symbol | Characteristic | 0°C | | | 25°C | | | 85°C | | | Unit |
|-------------|--|-------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | | 121 | 145 | | 121 | 145 | | 121 | 145 | mA |
| V_{OH} | Output HIGH Voltage (Note 2) | -1020 | -930 | -840 | -980 | -895 | -810 | -910 | -815 | -720 | mV |
| V_{OL} | Output LOW Voltage (Note 2) | -1950 | -1790 | -1630 | -1950 | -1790 | -1630 | -1950 | -1773 | -1595 | mV |
| V_{IH} | Input HIGH Voltage (Single-Ended) | -1170 | -1005 | -840 | -1130 | -970 | -810 | -1060 | -890 | -720 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) | -1950 | -1715 | -1480 | -1950 | -1715 | -1480 | -1950 | -1698 | -1445 | mV |
| V_{BB} | Output Voltage Reference | -1.38 | | -1.27 | -1.35 | | -1.25 | -1.31 | | -1.19 | V |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3) | -2.8 | | -0.4 | -2.8 | | -0.4 | -2.8 | | -0.4 | V |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current | 0.5 | 0.3 | | 0.5 | 0.065 | | 0.3 | 0.2 | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary $-0.46\text{ V} / +0.06\text{ V}$.
2. Outputs are terminated through a $50\ \Omega$ resistor to $V_{CC} - 2.0\text{ V}$.
3. V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} .

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Table 6. 100E SERIES PECL DC CHARACTERISTICS ($V_{CCx} = 5.0\text{ V}$; $V_{EE} = 0.0\text{ V}$ (Note 1))

| Symbol | Characteristic | 0°C | | | 25°C | | | 85°C | | | Unit |
|-------------|--|------|------|------|------|------|------|------|------|------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | | 121 | 145 | | 121 | 145 | | 139 | 167 | mA |
| V_{OH} | Output HIGH Voltage (Note 2) | 3975 | 4050 | 4120 | 3975 | 4050 | 4120 | 3975 | 4050 | 4120 | mV |
| V_{OL} | Output LOW Voltage (Note 2) | 3190 | 3295 | 3380 | 3190 | 3255 | 3380 | 3190 | 3260 | 3380 | mV |
| V_{IH} | Input HIGH Voltage (Single-Ended) | 3835 | 3975 | 4120 | 3835 | 3975 | 4120 | 3835 | 3975 | 4120 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) | 3190 | 3355 | 3525 | 3190 | 3355 | 3525 | 3190 | 3355 | 3525 | mV |
| V_{BB} | Output Voltage Reference | 3.62 | | 3.73 | 3.62 | | 3.74 | 3.62 | | 3.74 | V |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3) | 2.2 | | 4.6 | 2.2 | | 4.6 | 2.2 | | 4.6 | V |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current | 0.5 | 0.3 | | 0.5 | 0.25 | | 0.5 | 0.2 | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary $-0.46\text{ V} / +0.8\text{ V}$.
2. Outputs are terminated through a $50\ \Omega$ resistor to $V_{CC} - 2.0\text{ V}$.
3. V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} .

Table 7. 100E SERIES NECL DC CHARACTERISTICS ($V_{CCx} = 0.0\text{ V}$; $V_{EE} = -5.0\text{ V}$ (Note 1))

| Symbol | Characteristic | 0°C | | | 25°C | | | 85°C | | | Unit |
|-------------|--|-------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | | 121 | 145 | | 121 | 145 | | 139 | 167 | mA |
| V_{OH} | Output HIGH Voltage (Note 2) | -1025 | -950 | -880 | -1025 | -950 | -880 | -1025 | -950 | -880 | mV |
| V_{OL} | Output LOW Voltage (Note 2) | -1810 | -1705 | -1620 | -1810 | -1745 | -1620 | -1810 | -1740 | -1620 | mV |
| V_{IH} | Input HIGH Voltage (Single-Ended) | -1165 | -1025 | -880 | -1165 | -1025 | -880 | -1165 | -1025 | -880 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) | -1810 | -1645 | -1475 | -1810 | -1645 | -1475 | -1810 | -1645 | -1475 | mV |
| V_{BB} | Output Voltage Reference | -1.38 | | -1.27 | -1.38 | | -1.26 | -1.38 | | -1.26 | V |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3) | -3.8 | | -0.4 | -3.8 | | -0.4 | -3.8 | | -0.4 | V |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current | 0.5 | 0.3 | | 0.5 | 0.25 | | 0.5 | 0.2 | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary $-0.46\text{ V} / +0.8\text{ V}$.
2. Outputs are terminated through a $50\ \Omega$ resistor to $V_{CC} - 2.0\text{ V}$.
3. V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} .

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Table 8. AC CHARACTERISTICS ($V_{CCx} = 5.0\text{ V}$; $V_{EE} = 0.0\text{ V}$ or $V_{CCx} = 0.0\text{ V}$; $V_{EE} = -5.0\text{ V}$ (Note 1))

| Symbol | Characteristic | 0°C | | | 25°C | | | 85°C | | | Unit |
|--------------------------------------|--|--|--|--|--|--|--|--|--|--|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| f_{COUNT} | Maximum Count Frequency | 1800 | 2200 | | 1800 | 2200 | | 1800 | 2200 | | MHz |
| t_{PLH} t_{PHL} | Propagation Delay to Output CLK to Q0 CLK to Q1 CLK to Q2 CLK to Q3 CLK to Q4 CLK to Q5 CLK to Q6 CLK to Q7 A_Start to Q0 MR to Q0 | 1300 1600 1950 2275 2625 2950 3250 3575 950 700 | 1700 2025 2425 2750 3125 3450 3775 4075 1325 1000 | 2150 2500 2925 3350 3750 4150 4450 4800 1700 1300 | 1300 1600 1950 2275 2625 2950 3250 3575 950 700 | 1700 2050 2450 2775 3150 3475 3800 4125 1325 1000 | 2150 2500 2925 3350 3750 4150 4450 4800 1700 1300 | 1350 1650 2025 2350 2700 3050 3375 3700 950 700 | 1750 2100 2500 2850 3225 3550 3925 4250 1325 1000 | 2200 2550 3000 3425 3825 4250 4600 4950 1700 1300 | ps |
| t_s | Setup Time (EN1, EN2) | 0 | -150 | | 0 | -150 | | 0 | -150 | | ps |
| t_h | Hold Time (EN1, EN2) | 300 | 150 | | 300 | 150 | | 300 | 150 | | ps |
| t_{RR} | Reset Recovery Time MR, A_Start | 400 | 200 | | 400 | 200 | | 400 | 200 | | ps |
| t_{PW} | Minimum Pulse Width CLK, MR, A_Start | 400 | | | 400 | | | 400 | | | ps |
| V_{PP} | Input Voltage Swing CLK/CLK (Differential Configuration) (Note 2) | 0.25 | | 1.0 | 0.25 | | 1.0 | 0.25 | | 1.0 | V |
| t_{JITTER} | Random Clock Jitter (RMS) | | < 1 | | | < 1 | | | < 1 | | ps |
| t_r t_f | Rise/Fall Times (20%–80%) Q0, Q1 Q2 to Q7 | 150 275 | | 400 600 | 150 275 | | 400 600 | 150 275 | | 400 600 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- 10 Series: V_{EE} can vary $-0.46\text{ V} / +0.06\text{ V}$.
100 Series: V_{EE} can vary $-0.46\text{ V} / +0.8\text{ V}$.
- Minimum input swing for which AC parameters are guaranteed. Full DC ECL output swings will be generated with only 50 mV input swings.

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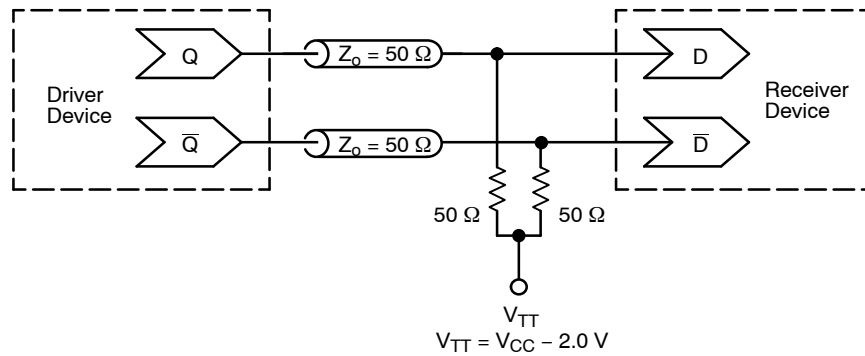


Figure 3. Typical Termination for Output Driver and Device Evaluation
(See Application Note [AND8020/D](#) – Termination of ECL Logic Devices.)

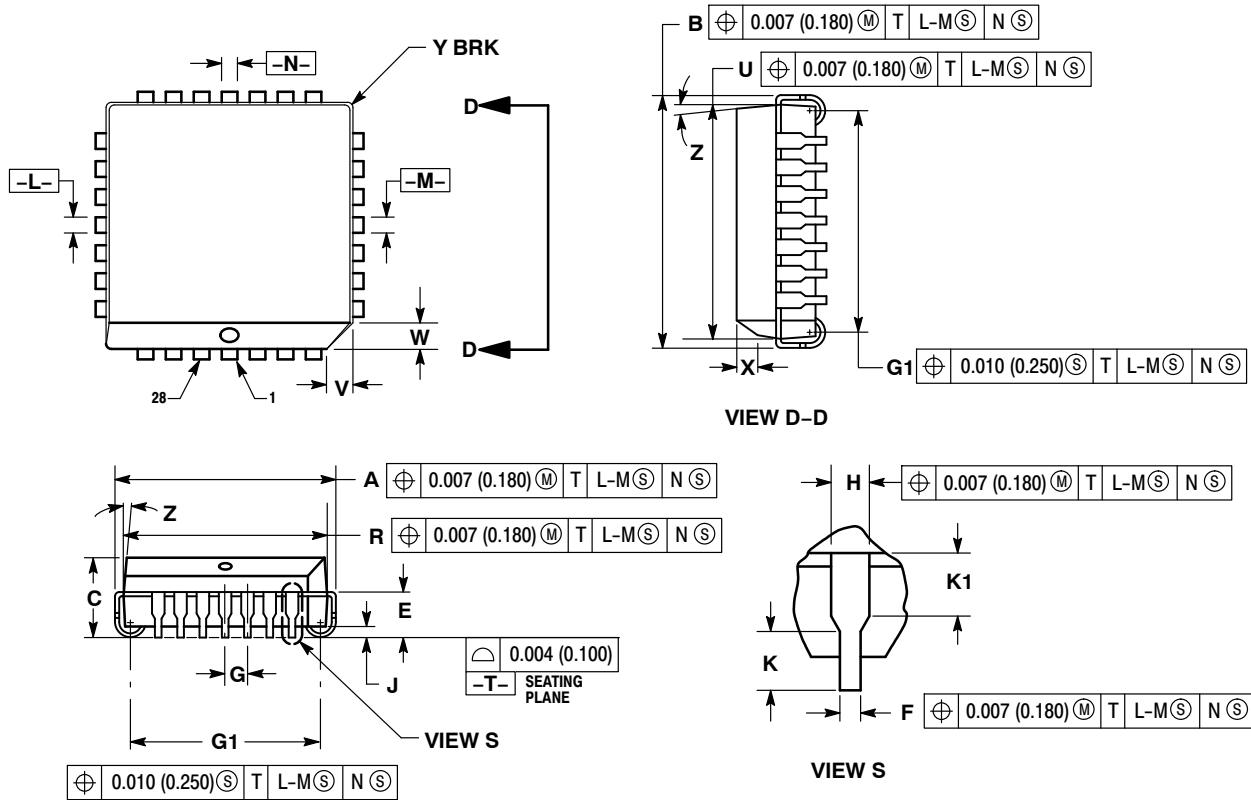
Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

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PACKAGE DIMENSIONS

28 LEAD PLCC
CASE 776-02
ISSUE F




NOTES:

- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
- DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
- DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.485 | 0.495 | 12.32 | 12.57 |
| B | 0.485 | 0.495 | 12.32 | 12.57 |
| C | 0.165 | 0.180 | 4.20 | 4.57 |
| E | 0.090 | 0.110 | 2.29 | 2.79 |
| F | 0.013 | 0.021 | 0.33 | 0.53 |
| G | 0.050 BSC | | 1.27 BSC | |
| H | 0.026 | 0.032 | 0.66 | 0.81 |
| J | 0.020 | --- | 0.51 | --- |
| K | 0.025 | --- | 0.64 | --- |
| R | 0.450 | 0.456 | 11.43 | 11.58 |
| U | 0.450 | 0.456 | 11.43 | 11.58 |
| V | 0.042 | 0.048 | 1.07 | 1.21 |
| W | 0.042 | 0.048 | 1.07 | 1.21 |
| X | 0.042 | 0.056 | 1.07 | 1.42 |
| Y | --- | 0.020 | --- | 0.50 |
| Z | 2° | 10° | 2° | 10° |
| G1 | 0.410 | 0.430 | 10.42 | 10.92 |
| K1 | 0.040 | --- | 1.02 | --- |

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